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10/754,565	01/12/2004	Chandra Mouli	M4065.0997/P997	8237

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EXAMINER	
LOKE, STEVEN HO YIN	

ART UNIT	PAPER NUMBER
2811	

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Please find below and/or attached an Office communication concerning this application or proceeding.

AK

Office Action Summary	Application No.	Applicant(s)
	10/754,565	MOULI, CHANDRA
	Examiner	Art Unit
	Steven Loke	2811

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 April 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-66* is/are pending in the application.

4a) Of the above claim(s) *43-66* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-40 and 42* is/are rejected.

7)☒ Claim(s) *41* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.

4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

5) ☐ Notice of Informal Patent Application (PTO-152)

6) ☐ Other: _____.

1. Applicant's election without traverse of claims 1-42 in the reply filed on 4/19/05 is acknowledged.

2. Figures 1 and 2 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

3. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(4) because reference character "36" has been used to designate both source follower transistor and row select transistor. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

4. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign(s) mentioned in the description: 38 (page 3, line 7). Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

5. Claims 10, 12 and 14 are objected to because of the following informalities: Claim 10, line 3, claim 12, line 3, the phrase "said STI region" has no antecedent basis. Claim 14, line 2, "said layer of high-k dielectric material" has no antecedent basis. Appropriate correction is required.

6. Claims 35, 36 and 38 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 35, line 3, the phrase "a second portion of said accumulation region of said" is not understood. Is it being referred to "a second portion of said accumulation region of said photodiode"?

Claim 38, line 4, the phrase "other insulating material" is vague and indefinite as to what is the other insulating material.

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 1-4, 39, 40 and 42 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nozaki et al. in view of Kim et al.

In regards to claim 1, Nozaki et al. disclose a pixel cell (RANGE A) in fig. 7. It comprises: a substrate [11]; a photosensor [34] in said substrate, said photosensor [34] including a first conductivity (n-type) area [15] below a surface of said substrate and a second conductivity (p-type) area [21] at least between said first conductivity area and said substrate surface.

Nozaki et al. differ from the claimed invention by not showing a first layer having an excess charge sufficient to create an electric field that affects said second conductivity area.

Kim et al. disclose a first layer [310] (paragraphs [0050]-[0051]) made of aluminum oxide formed in an isolation trench [318] in fig. 9. It is well known in the art that aluminum oxide having fixed (negative) charges (See the 7^{th} paragraph in page 525 of Sazonov et al.).

Since both Nozaki et al. and Kim et al. teach an isolation trench, it would have been obvious to have the isolation trench of Kim et al. in Nozaki et al. because it can reduce

the consumption of the silicon substrate. The combined device further discloses the negative charges in the aluminum oxide are able to create an electric field that affects said second conductivity area of the photosensor.

In regards to claim 2, Nozaki et al. further disclose said photosensor is a pinned photodiode.

In regards to claim 3, the combined device further discloses an isolation region (the STI region adjacent to the layer [24a]) spaced from said photosensor, wherein said isolation region has a bottom and sidewalls with said first layer deposited thereon.

In regards to claim 4, Nozaki et al. further disclose a second layer [25] on a surface of said substrate over said isolation region and said photosensor.

In regards to claim 39, Nozaki et al. teach a pixel cell (RANGE A) in fig. 7. It comprising: a photodiode [34] in a substrate [11]; an isolation trench (STI) in said substrate and having a bottom and sidewalls adjacent to said photodiode.

Nozaki et al. differ from the claimed invention by not showing a layer of silicon dioxide on said bottom and said sidewalls of said isolation trench and a layer of aluminum oxide over said layer of silicon dioxide.

Kim et al. teach a layer of silicon dioxide [308] on said bottom and said sidewalls of said isolation trench [318] and a layer of aluminum oxide [310] over said layer of silicon dioxide in fig. 9.

Since both Nozaki et al. and Kim et al. teach an isolation trench, it would have been obvious to have the isolation trench of Kim et al. in Nozaki et al. because it can reduce the consumption of the silicon substrate.

In regards to claim 40, Nozaki et al. further disclose a layer of silicon dioxide [12] on a surface of said substrate over said photodiode.

In regards to claim 42, Kim et al. further disclose a part of said isolation trench is filled with aluminum oxide [310].

9. Claims 30-34, 37 and 38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Prior art (fig. 1) in view of Nozaki et al., further in view of Kim et al.

In regards to claim 30, Prior art (fig. 1) discloses an imager device [100]. It comprising: an image processor [180]; and a pixel array [110] for supplying signals to said image processor.

Prior art (fig. 1) differ from the claimed invention by not showing at least one pixel of said array comprising: a substrate; a photodiode within said substrate; an isolation trench within said substrate; and a lining layer in said isolation trench comprising a layer of high-k dielectric material; and a surface layer on a surface of said substrate located over said photodiode, comprising a layer of high-k dielectric material.

Nozaki et al. disclose a pixel of an image sensor in fig. 7. It comprising: a substrate [11]; a photodiode [34] within said substrate; an isolation trench (STI) within said substrate; and a surface layer [17] on a surface of said substrate located over said photodiode, comprising a layer of high-k dielectric material (silicon nitride).

Since both Prior art (fig. 1) and Nozaki et al. teach an image device, it would have been obvious to have the pixel structure of Nozaki et al. in Prior art (fig. 1) because it is a widely used pixel structure in an image device.

Nozaki et al. further differ from the claimed invention by not showing a lining layer in said isolation trench comprising a layer of high-k dielectric material.

Kim et al. teach a lining layer [310] in said isolation trench [318] comprising a layer of high-k dielectric material (aluminum oxide) in fig. 9.

Since both Nozaki et al. and Kim et al. teach an isolation trench, it would have been obvious to have the isolation trench of Kim et al. in Nozaki et al. because it can reduce the consumption of the silicon substrate.

In regards to claim 31, the combined device further disclose a dielectric layer (layer [308] of Kim et al. and layer [12] of Nozaki et al.) between said isolation trench and said lining layer [310].

In regards to claim 32, the combined device further disclose said dielectric layer extends over said surface of said substrate, between said surface layer and said surface of said substrate.

In regards to claim 33, the combined device further discloses said dielectric layer comprises silicon dioxide.

In regards to claim 34, it is well known in the art that the combined device shows said lining layer has an excess charge sufficient to maintain a field in a first portion of an accumulation region ([21] of Nozaki et al.) of said photodiode.

In regards to claim 37, Kim et al. further disclose a filling layer [316] located over said lining layer [310], filling said isolation trench.

In regards to claim 38, Kim et al. further disclose said filling layer [316] is silicon dioxide (BPSG).

10. Claims 1-10, 14, 16-23, 29, 30 and 34-36 are rejected under 35 U.S.C. 103(a) as being obvious over Mouli et al. in view of Kim et al.

The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art only under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 103(a) might be overcome by: (1) a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not an invention "by another"; (2) a showing of a date of invention for the claimed subject matter of the application which corresponds to subject matter disclosed but not claimed in the reference, prior to the effective U.S. filing date of the reference under 37 CFR 1.131; or (3) an oath or declaration under 37 CFR 1.130 stating that the application and reference are currently owned by the same party and that the inventor named in the application is the prior inventor under 35 U.S.C. 104, together with a terminal disclaimer in accordance with 37 CFR 1.321(c). This rejection might also be overcome by showing that the reference is disqualified under 35 U.S.C. 103(c) as prior art in a rejection under 35 U.S.C. 103(a). See MPEP § 706.02(l)(1) and § 706.02(l)(2).

In regards to claim 1, Mouli et al. disclose a pixel cell [410] in fig. 4. It comprises: a substrate [420]; a photosensor [421] in said substrate, said photosensor [421] including a first conductivity (n-type) area [426] below a surface of said substrate and a second conductivity (p-type) area [424] at least between said first conductivity area and said substrate surface.

Mouli et al. differ from the claimed invention by not showing a first layer having an excess charge sufficient to create an electric field that affects said second conductivity area.

Kim et al. disclose a first layer [310] (paragraphs [0050]-[0051]) made of aluminum oxide formed in an isolation trench [318] in fig. 9. It is well known in the art that aluminum oxide having fixed (negative) charges (See the 7th paragraph in page 525 of Sazonov et al.) that would affect its surrounding area.

Since both Mouli et al. and Kim et al. teach an isolation trench, it would have been obvious to have the isolation trench of Kim et al. in Mouli et al. because it can reduce the consumption of the silicon substrate. The combined device further discloses the negative charges in the aluminum oxide are able to create an electric field that affects said second conductivity area of the photosensor.

In regards to claim 2, Mouli et al. further disclose said photosensor is a pinned photodiode.

In regards to claim 3, the combined device further discloses an isolation region spaced from said photosensor, wherein said isolation region has a bottom and sidewalls with said first layer deposited thereon.

In regards to claim 4, Mouli et al. further disclose a second layer [461] on a surface of said substrate over said isolation region and said photosensor.

In regards to claim 5, Mouli et al. inherently disclose said second layer (aluminum oxide) (an upper portion of layer [461]) has an excess charge sufficient to create an electric field which affects said second conductivity area. It is well known in the art that

aluminum oxide having fixed (negative) charges (See the 7th paragraph in page 525 of Sazonov et al.) that would affect its surrounding area.

In regards to claim 6, the combined device shows said first and second layers comprise a high-k dielectric material.

In regards to claim 7, the combined device shows said high-k dielectric material has an excess negative charge.

In regards to claim 8, the combined device shows said high-k dielectric is aluminum oxide.

In regards to claim 9, the combined device inherently teaches said second conductivity area maintains holes at said substrate surface and at a surface of said isolation region sidewall because the negative charges of the aluminum oxide layers attract holes from the second conductivity (p-type) area and the p-type substrate.

In regards to claim 10, the combined device inherently teaches said field prevents a depletion region of said photodiode from reaching at least one of said STI region and said substrate surface because there are excess negative charges near the STI region and the substrate surface.

In regards to claim 14, Mouli et al. teach a dielectric layer (a lower portion of layer [461]) between said layer of high-k dielectric material and said substrate.

In regards to claim 16, Mouli et al. teach a pixel cell [410]. It comprising: a substrate [420] having a first conductivity type (p-type); a pinned photodiode [421] in said substrate and having a charge collection region [426] of a second conductivity type (n-type) and an accumulation region [424] of said first conductivity type at least over said

charge collection region; and a surface of said substrate inherently has a charge density (from the negative charges of the aluminum oxide layer [461]) sufficient to maintain an electric field in an adjacent portion of said accumulation region.

Mouli et al. differ from the claimed invention by not showing an isolation trench adjacent to said pinned photodiode, wherein sidewalls of said isolation trench have a charge density sufficient to maintain an electric field in an adjacent portion of said accumulation region.

Kim et al. teach an isolation trench [318] and sidewalls of said isolation trench have a charge density (from the negative charges of the aluminum oxide layer [461]) in fig. 9.

Since both Mouli et al. and Kim et al. teach an isolation trench in a semiconductor substrate, it would have been obvious to have the isolation trench of Kim et al. in Mouli et al. because it can reduce the consumption of the silicon substrate. The combined device shows an isolation trench adjacent to said pinned photodiode, wherein sidewalls of said isolation trench have a charge density (from the negative charges of the aluminum oxide layer [461]) sufficient to maintain an electric field in an adjacent portion of said accumulation region.

In regards to claim 17, the combined device shows said sidewalls and said surface of said substrate (an upper portion of layer [461] in Mouli et al.) each comprise a layer of high-k dielectric material (aluminum oxide).

In regards to claim 18, Mouli et al. show said first conductivity type is p-type and said second conductivity type is n-type.

In regard to claim 19, the combined device teaches said charge density is negative charge density.

In regards to claim 20, the combined device teaches said layers of high-k dielectric material have an excess negative charge (the fixed negative charge in aluminum oxide).

In regards to claim 21, the combined device teaches said high-k dielectric material is aluminum oxide.

In regards to claim 22, Kim et al. teach a portion of said isolation trench [318] is filled with a high-k dielectric material having an excess negative charge (the fixed negative charge in aluminum oxide).

In regards to claim 23, the combined device further discloses said sidewalls and said surface of said substrate further comprise a layer of dielectric material ([layer [308] of Kim et al. and the lower portion of layer [461] in Mouli et al.) between said layer of high-k dielectric material and said substrate.

In regards to claim 29, Kim et al. further disclose a silicon dioxide layer [308] in contact with said substrate [300].

In regards to claim 30, Mouli et al. teach an imager device in figs. 4 and 7. It comprising: an image processor [744]; and a pixel array [742] for supplying signals to said image processor, at least one pixel of said array (fig. 4) comprising: a substrate [420]; a photodiode [421] within said substrate; and a surface layer [461] on a surface of said substrate located over said photodiode, comprising a layer of high-k dielectric material (aluminum oxide).

Mouli et al. differ from the claimed invention by not showing an isolation trench within said substrate and a lining layer in said isolation trench comprising a layer of high-k dielectric material.

Kim et al. teach an isolation trench [318] within a substrate [300] and a lining layer [310] in said isolation trench [318] comprising a layer of high-k dielectric material (aluminum oxide) in fig. 9.

Since both Mouli et al. and Kim et al. teach an isolation trench, it would have been obvious to have the isolation trench of Kim et al. in Mouli et al. because it can reduce the consumption of the silicon substrate.

In regards to claim 34, Kim et al. inherently shows said lining layer has an excess charge (the fixed negative charge in aluminum oxide) sufficient to maintain a field in a first portion of an accumulation region ([424] of Mouli et al.) of said photodiode.

In regards to claim 35, Mouli et al. inherently teach said surface layer has an excess charge (the fixed negative charge in aluminum oxide) sufficient to maintain a field in a second portion of said accumulation region of said photodiode.

In regards to claim 36, the combined device teaches said lining layer and said surface layer are high-k dielectric materials made of aluminum oxide.

11. Claims 1-6, 11-17 and 23-28 are rejected under 35 U.S.C. 103(a) as being obvious over Mouli et al. in view of Benedict et al.

The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art only under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 103(a) might be overcome

by: (1) a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not an invention "by another"; (2) a showing of a date of invention for the claimed subject matter of the application which corresponds to subject matter disclosed but not claimed in the reference, prior to the effective U.S. filing date of the reference under 37 CFR 1.131; or (3) an oath or declaration under 37 CFR 1.130 stating that the application and reference are currently owned by the same party and that the inventor named in the application is the prior inventor under 35 U.S.C. 104, together with a terminal disclaimer in accordance with 37 CFR 1.321(c). This rejection might also be overcome by showing that the reference is disqualified under 35 U.S.C. 103(c) as prior art in a rejection under 35 U.S.C. 103(a). See MPEP § 706.02(l)(1) and § 706.02(l)(2).

In regards to claim 1, Mouli et al. discloses a pixel cell [410] in fig. 4. It comprises: a substrate [420]; a photosensor [421] in said substrate, said photosensor [421] including a first conductivity (p-type) (paragraph [0055]) area [426] below a surface of said substrate and a second conductivity (n-type) (paragraph [0055]) area [424] at least between said first conductivity area and said substrate surface.

Mouli et al. differ from the claimed invention by not showing a first layer having an excess charge sufficient to create an electric field that affects said second conductivity area.

Benedict et al. disclose a first layer [20] made of silicon oxynitride formed in an isolation trench [16] in fig. 1F. It is well known in the art that silicon oxynitride having

fixed (positive) charges (See the Introduction in Novkovski) that would affect its surrounding area.

Since both Mouli et al. and Benedict et al. teach an isolation trench, it would have been obvious to have the isolation trench of Benedict et al. in Mouli et al. because it prevents diffusion of oxygen into the semiconductor substrate. The combined device further discloses the positive charges in the silicon oxynitride are able to create an electric field that affects said second conductivity area of the photosensor.

In regards to claim 2, Mouli et al. further disclose said photosensor is a pinned photodiode.

In regards to claim 3, the combined device further discloses an isolation region spaced from said photosensor, wherein said isolation region has a bottom and sidewalls with said first layer deposited thereon.

In regards to claim 4, Mouli et al. further disclose a second layer [461] on a surface of said substrate over said isolation region and said photosensor.

In regards to claim 5, Mouli et al. inherently disclose said second layer (silicon oxynitride) (an upper portion of layer [461]) has an excess charge sufficient to create an electric field which affects said second conductivity area. It is well known in the art that silicon oxynitride having fixed (positive) charges (See the Introduction in Novkovski) that would affect its surrounding area.

In regards to claim 6, the combined device shows said first and second layers comprise a high-k dielectric material (silicon oxynitride).

In regards to claim 11, the combined device teaches said high-k dielectric material has an excess positive charge (the fixed positive charge in silicon oxynitride).

In regards to claim 12, the combined device inherently teaches said second conductivity area maintains electrons at said substrate surface and at a surface of said STI region sidewall because the positive charges attract the electrons to the substrate surface and the sidewall of the substrate near the isolation trench.

In regards to claim 13, the Mouli et al. inherently teach said second conductivity area accumulates electrons because the positive charges attract the electrons in the second conductivity area.

In regards to claim 14, Mouli et al. teach a dielectric layer (a lower portion of layer [461]) between said layer of high-k dielectric material and said substrate.

In regards to claim 15, Mouli et al teach said dielectric layer comprises silicon dioxide (silicon oxynitride comprises silicon dioxide).

In regards to claim 16, Mouli et al. teach a pixel cell [410]. It comprising: a substrate [420] having a first conductivity type (n-type) (paragraph [0055]); a pinned photodiode [421] in said substrate and having a charge collection region [426] of a second conductivity type (p-type) (paragraph [0055]) and an accumulation region [424] of said first conductivity type at least over said charge collection region; and a surface of said substrate inherently has a charge density (from the positive charges of the silicon oxynitride layer [461]) sufficient to maintain an electric field in an adjacent portion of said accumulation region.

Mouli et al. differ from the claimed invention by not showing an isolation trench adjacent to said pinned photodiode, wherein sidewalls of said isolation trench have a charge density sufficient to maintain an electric field in an adjacent portion of said accumulation region.

Benedict et al. teach an isolation trench [16] and sidewalls of said isolation trench have a charge density (from the positive charges of the silicon oxynitride layer [20]) in fig. 1F.

Since both Mouli et al. and Benedict et al. teach an isolation trench in a semiconductor substrate, it would have been obvious to have the isolation trench of Benedict et al. in Mouli et al. because it prevents diffusion of oxygen into the semiconductor substrate. The combined device shows an isolation trench adjacent to said pinned photodiode, wherein sidewalls of said isolation trench have a charge density (from the positive charges of the silicon oxynitride layer [20) sufficient to maintain an electric field in an adjacent portion of said accumulation region.

In regards to claim 17, the combined device shows said sidewalls and said surface of said substrate (an upper portion of layer [461] in Mouli et al.) each comprise a layer of high-k dielectric material (silicon oxynitride).

In regards to claim 23, the combined device further discloses said sidewalls and said surface of said substrate further comprise a layer of dielectric material ([layer [18] of Benedict et al. and the lower portion of layer [461] in Mouli et al.) between said layer of high-k dielectric material and said substrate.

In regards to claim 24, the combined device teaches said dielectric material comprises silicon dioxide.

In regards to claim 25, Mouli et al. further disclose said first conductivity type is n-type and said second conductivity is p-type.

In regards to claim 26, the combined device teaches said charge density is positive charge density.

In regards to claim 27, the combined device teaches said layers of high-k dielectric material have an excess positive charge (the fixed positive charge in silicon oxynitride).

In regards to claim 28, Benedict et al. further disclose a part of said isolation trench is filled with a high-k dielectric material having an excess positive charge (the fixed positive charge in silicon oxynitride).

12. Claim 41 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

13. The following is a statement of reasons for the indication of allowable subject matter: The major difference in the claims not found in the prior art of record is a layer of aluminum oxide over said layer of silicon dioxide on said substrate surface.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Steven Loke whose telephone number is (571) 272-1657. The examiner can normally be reached on 8:20 am to 5:50 pm.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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June 26, 2005

Steven Loke
Primary Examiner
Steven Loke